

WHAT IS CLAIMED IS:

1           1.       An integrated circuit, comprising:  
2           a programmable logic portion;  
3           a first JTAG circuit, wherein the first JTAG circuit comprises a first TAP  
4 controller coupled to a first instruction register and a first plurality of data registers; and  
5           an embedded logic portion comprising a processor and a second JTAG circuit  
6 coupled to the first JTAG circuit and to the processor, wherein the second JTAG circuit  
7 comprises a second TAP controller coupled to a second instruction register and a second  
8 plurality of data registers.

1           2.       The integrated circuit of claim 1 wherein one of the first plurality of  
2 data registers comprises a data register that is used to load data into the programmable logic  
3 portion to configure logic circuitry in the programmable logic portion.

1           3.       The integrated circuit of claim 1 wherein one of the first plurality of  
2 data registers comprises a data register that is allows a user to transmit and receive data from  
3 the programmable logic portion.

1           4.       The integrated circuit of claim 1 wherein one of the second plurality of  
2 data registers comprises a first data register that acts as a communications interface between  
3 the embedded logic portion of the integrated circuit and an external host processor.

1           5.       The integrated circuit of claim 4 wherein the external host processor  
2 loads first action bits into the first data register indicating a first action to be performed by  
3 circuitry in the embedded logic portion, and wherein second action bits may not be loaded  
4 into the first data register until the first action has been performed and the first data register  
5 has communicated results of the first action to the external host processor.

1           6.       The integrated circuit of claim 4 wherein the external host processor  
2 selects a variable length scan chain as the first data register.

1           7.       The integrated circuit of claim 6 wherein the variable length scan chain  
2 is synchronized between the external host processor and the processor in the embedded logic  
3 portion using a particular pattern of ones and zeros.

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1                   8.       The integrated circuit of claim 7 wherein the particular pattern of ones  
2 and zeros is one bit long and has a value of one.

1                   9.       The integrated circuit of claim 1 wherein the second plurality of data  
2 registers are coupled to a first multiplexer that is controlled by data signals decoded from the  
3 second instruction register.

1                   10.      The integrated circuit of claim 9 wherein an output of the first  
2 multiplexer, the second instruction register, and a test data output of the first JTAG circuit are  
3 coupled to a second multiplexer that is controlled by the second TAP controller.

1                   11.      An embedded logic portion of an integrated circuit, the integrated  
2 circuit comprising a programmable logic portion, the embedded logic portion comprising:  
3                   a processor; and  
4                   a first JTAG circuit coupled to the processor and a second JTAG circuit that is  
5 part of control logic for the programmable logic portion, wherein the first JTAG circuit  
6 comprises a first TAP controller that outputs a plurality of control signals that control a first  
7 instruction register and a first plurality of data registers.

1                   12.      The embedded logic portion of claim 11 wherein the second JTAG  
2 circuit comprises a second plurality of data registers coupled to a second TAP controller, and  
3 wherein one of the second plurality of data registers comprises a bypass register that does not  
4 perform any function.

1                   13.      The embedded logic portion of claim 11 wherein the second JTAG  
2 circuit comprises a second plurality of data registers coupled to a second TAP controller, and  
3 wherein one of the second plurality of data registers comprises a data register that can force  
4 data onto and capture data from a plurality of input/output pins.

1                   14.      The embedded logic portion of claim 11 wherein the second JTAG  
2 circuit comprises a second plurality of data registers coupled to a second TAP controller, and  
3 wherein one of the second plurality of data registers comprises a data register that is used to  
4 load data into the programmable logic portion to configure logic circuitry in the  
5 programmable logic portion.

1           15.     The embedded logic portion of claim 11 wherein the second JTAG  
2 circuit comprises a second plurality of data registers coupled to a second TAP controller, and  
3 wherein one of the second plurality of data registers comprises a data register that allows a  
4 user to transmit and receive data from the programmable logic portion on input/output pins.

1           16.     The embedded logic portion of claim 11 wherein one of the first  
2 plurality of data registers comprises a first data register that acts as a communications  
3 interface between the embedded logic portion and an external host processor.

1           17.     The embedded logic portion of claim 16 wherein the external host  
2 processor loads first action bits into the first data register indicating a first action to be  
3 performed by circuitry in the embedded logic portion, and wherein second action bits may  
4 not be loaded into the first data register until the first action has been performed and the first  
5 data register has communicated results of the first action to the external host processor.

1           18.     The embedded logic portion of claim 16 wherein the external host  
2 processor selects a variable length scan chain as the first data register.

1           19.     The embedded logic portion of claim 11 wherein the first plurality of  
2 data registers are coupled to a first multiplexer that is controlled by data signals decoded from  
3 the first instruction register.

1           20.     The embedded logic portion of claim 19 wherein an output of the first  
2 multiplexer, the first instruction register, and a test data output of the second JTAG circuit are  
3 coupled to a second multiplexer that is controlled by the first TAP controller.

1           21.     A method for testing data using a chip that comprises a first processor  
2 and a programmable logic portion, comprising:  
3           transmitting first data signals between pins and circuitry in the programmable  
4 logic portion using a first JTAG circuit; and  
5           transmitting second data signals between an external host processor and the  
6 first processor using a second JTAG circuit in an embedded logic portion of the chip.

1           22.     The method of claim 21 wherein the first and second JTAG circuits  
2 comprise first and second TAP controllers, respectively.

1           23.     The method of claim 21 wherein transmitting the first data signals  
2 further comprises loading the first data signals into the programmable logic portion to  
3 configure logic circuitry in the programmable logic portion using a data register that is part of  
4 the first JTAG circuit. circuit.

1           24.     The method of claim 21 wherein transmitting the second data signals  
2 further comprises transmitting the second data signals between the external host processor  
3 and the embedded logic portion using a data register that is part of the second JTAG circuit.

1           25.     The method of claim 21 transmitting the second data signals further  
2 comprises selecting from a plurality of data registers in the second JTAG circuit using a first  
3 multiplexer that is controlled by signals decoded from an instruction register.

1           26.     The method of claim 25 wherein transmitting the second data signals  
2 further comprises selecting from an output of the first multiplexer, an output of the  
3 instruction register, and a test data output of the first JTAG circuit using a second multiplexer  
4 that is controlled by a TAP controller in the second JTAG circuit.

1           27.     An integrated circuit, comprising:  
2                 a processor comprising a first JTAG circuit, wherein the first JTAG circuit  
3 comprises a first TAP controller coupled to a first instruction register and a first plurality of  
4 data registers; and  
5                 a second JTAG circuit coupled to the first JTAG circuit, wherein the second  
6 JTAG circuit comprises a second TAP controller coupled to a second instruction register and  
7 a second plurality of data registers.

1           28.     The integrated circuit of claim 27 wherein the integrated circuit  
2 comprises an embedded logic portion and a programmable logic portion, and wherein the  
3 second JTAG circuit is part of an embedded logic portion of the integrated circuit.

1           29.     The integrated circuit of claim 28 wherein the second JTAG circuit  
2 comprises a multiplexer having a first input coupled to an output of the first JTAG circuit and  
3 a second input coupled to receive data signals from one of the second plurality of data  
4 registers.